8. In an electroluminescent display comprising an array of pixels, where each pixel contains a circuit for controlling application of energy to an electroluminescent cell associated with each pixel in said array of pixels, a method of providing gray scale illumination during a frame period comprising the steps of:

dividing said frame period into a plurality of LOAD periods and a plurality of ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period;

applying, during each of said LOAD periods, a data signal to said circuit along a data line and applying a select signal to said circuit along a select line;

storing, during each of said LOAD periods, said data line signal within said circuit; and

applying, during each of said ILLUMINATE periods, a current to said electroluminescent cell and said circuit, where said electroluminescent cell is selectively illuminated in response to said current and said stored data line signal.

9. The method of claim 8 wherein, during said ILLUMINATE periods, said method further comprises the steps of:

applying a gray scale control signal to said data line; and

applying said current to said electroluminescent cell when said gray scale control signal has a magnitude value that is less than said stored data signal.

10. The method of claim 9 wherein said gray scale control signal has a linear ramp waveform over the plurality of ILLUMINATE ILLUMINATION periods within one frame period.

11. The method of claim 9 wherein said gray scale control signal has a stepped waveform over the plurality of ILLUMINATION periods within one frame period, where each step in the waveform corresponds to one ILLUMINATION period.

12. The method of claim 8 wherein said data signal is a digital signal containing a plurality of bits where each bit is applied to said circuit during a plurality of consecutive LOAD periods.

13. The method of claim 12 wherein a significance of each bit of said data signal corresponds to an amount of energy applied to said electroluminescent cell during each ILLUMINATE period that follows the LOAD period in which each bit is applied to the circuit.

14. An electroluminescent display comprising an array of pixels, each pixel comprising:

a first transistor and a second transistor;

said first transistor having a first transistor gate, a first transistor source and a first transistor drain, where said first transistor gate is connected to a select line, said first transistor source is connected to a data line and said first transistor drain is connected to a second transistor gate of said second transistor;

said second transistor having said second transistor gate, a second transistor source and a second transistor drain, where said second transistor source is connected to said data line and second transistor drain is connected to an electroluminescent cell;

during a LOAD period and when a select line signal on the select line activates the first transistor, said data line supplies, through said first transistor, a data signal to the second transistor gate where said data signal is stored; and

during an ILLUMINATE period, said data line supplies a gray scale control signal to said second transistor, when said data signal stored at said second transistor gate exceeds the gray scale control signal on said data line, said second transistor applies energy from a power supply to said electroluminescent cell.

15. The display of claim 14 wherein said gray scale control signal has a ramp waveform over the ILLUMINATE period.

16. The display of claim 14 wherein said gray scale control signal has a step waveform over the ILLUMINATE period.

17. The display of claim 14 wherein a frame period is divided into a plurality of LOAD periods and ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period.

18. The display of claim 14 wherein said gray scale control signal has a ramp waveform over the plurality of ILLUMINATE periods.

19. The display of claim 14 wherein said gray scale control signal has a step waveform, where each step in said step waveform is coincident with one ILLUMINATE period in said plurality of ILLUMINATE periods.

20. An electroluminescent display comprising an array of pixels, each pixel comprising:

a control circuit, connected to a select line, a data line and a first electrode of an electroluminescent cell, for selectively applying energy to said electroluminescent cell in response to signals carried by said select line and said data line;

during a LOAD period and when a select line signal on the select line activates the control circuit, said data line supplies a data signal to the control circuit where said data signal is stored; and

during an ILLUMINATE period, in response to a state of said stored data signal, said control circuit applies pulsed energy from a power supply means to a second electrode of said electroluminescent cell for a particular period of time.

21. The display of claim 20 wherein a frame period is divided into a plurality of LOAD periods and ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period.

22. The display of claim 21 wherein a number of ILLUMINATE periods and LOAD periods that are used to illuminate said electroluminescent cell during a frame period is equivalent to a number of bits in said data signal.

23. The display of claim 22 wherein said data signal contains a plurality of bits, where, during each LOAD period, one of said plurality of bits in said data signal having a particular significance is stored in said control circuit and, during each ILLUMINATE period following said LOAD period, the significance of the stored bit corresponds to a number of pulses of energy from said series of energy pulses that are supplied to said electroluminescent cell through said control circuit.

24. The display of claim 23 wherein a state of the stored bit determines whether or not the number of energy pulses is applied to the electroluminescent cell during the associated ILLUMINATE period.

25. The display of claim 20 wherein said control circuit further comprises:

a first transistor and a second transistor;

said first transistor having a first transistor gate, a first transistor source and a first transistor drain, where said first transistor gate is connected to a select line, said first transistor source is connected to a data line and said first transistor drain is connected to a second transistor gate of said second transistor; and

said second transistor having said second transistor gate, a second transistor source and a second transistor drain, where said second transistor source is connected to said data line and second

transistor drain is connected to a first electrode of an electroluminescent cell.

26. The display of claim 20 wherein a frame period is divided into a plurality of LOAD periods and ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period.

27. The display of claim 26 wherein a number of ILLUMINATE periods and LOAD periods that are used to illuminate said electroluminescent cell during a frame period is equivalent to a number of bits in said data signal.

28. The display of claim 27 wherein said data signal contains a plurality of bits, where, during each LOAD period, one of said plurality of bits in said data signal having a particular significance is stored in said control circuit and, during each ILLUMINATE period following said LOAD period, the significance of the stored bit corresponds to a number of pulses of energy from said series of energy pulses that are supplied to said electroluminescent cell through said control circuit.

29. The display of claim 28 wherein a state of the stored bit determines whether or not the number of energy pulses is applied to the electroluminescent cell during the associated ILLUMINATE period.

30. An electroluminescent display comprising an array of pixels, each pixel comprising:

a first transistor, a second transistor and an electroluminescent cell;

said first transistor having a first transistor gate connected to a select line, a first transistor source connected to a data line, and a first transistor drain connected to connected to a second transistor gate of said second transistor;

said second transistor having a second transistor source connected to said data line and a second transistor drain coupled to a first electrode of said electroluminescent cell; and

said electroluminescent cell having a second electrode coupled to means for providing an alternating current to the electroluminescent cell.

31. The display of claim 30 further comprising:

a first capacitor, connected between said second transistor drain and said first electrode of said electroluminescent cell, for coupling said second transistor to said electroluminescent cell.

32. The display of claim 30 further comprising:

a second capacitor, connected between said second electrode of said electroluminescent cell and said means for providing an alternating current, for coupling said electroluminescent cell to said means for providing alternating current.